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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/677,698
Filing Date	September 28, 2000
First Named Inventor	Rajendran Nair
Art Unit	2814
Examiner Name	Shrinivas H. Rao
Total Number of Pages in This Submission: 65	Attorney Docket Number: 42390.P9239

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form (2 copies)
- [x] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance communication to Technology Center (TC)
- [x] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) (please Identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Dennis A. Nicholls Reg. No. 42,036
Signature	Dennis A. Nicholls
Date	November 19, 2003

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Typed or printed name	Anne Collette		
Signature	Anne Collette	Date	November 19, 2003

PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	09/677,698
Filing Date	September 28, 2000
First Named Inventor	Rajendran Nair
Examiner Name	Shrinivas H. Rao
Art Unit	2814
Attorney Docket No.	42390.P9239

METHOD OF PAYMENT *(check all that apply)*

☑ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

The Director is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☑ Credit any overpayments

☑ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X	=
Independent Claims		-3** =		X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330.00

SUBMITTED BY

(Complete *(if applicable)*)

Name *(Print/Type)*	Dennis A. Nicholls	Registration No. *(Attorney/Agent)*	42,036	Telephone	408-720-8300
Signature	Dennis A. Nicholls			Date	November 19, 2003

WARNING: Information on this form may become public. Credit card information should not be included in this form. Provide credit card information and authorization on PTO-2038.

Docket No.: 42390.P9239

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re the application of:	)	
	)	
Nair, Rajendran, et al.	)	
	)	
Serial No.: 09/677,698	)	Examiner: Rao, S.
	)	
Filed: 09/28/ 2000	)	Art Unit: 2814
	)	
For: METHOD AND APPARATUS FOR WEAK INVERSION MODE MOS DECOUPLING CAPACITOR	)	

APPELLANTS' BRIEF UNDER 37 CFR § 1.192
IN SUPPORT OF APPELLANTS' APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Hon. Commissioner for Patents
Mail Stop Appeal Brief – Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants hereby submit this Brief in triplicate in support of an appeal from a final decision of the Examiner, in the above-referenced case. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interference for allowance of the above-referenced patent application.

TABLE OF CONTENTS

I. Real Party in Interest

The real party in interest in the present appeal is Intel Corporation, a Delaware Corporation headquartered in Santa Clara, California, the assignee of the present application.

II. Related Appeals and Interferences

There are no related appeals or interferences to appellants' knowledge that would have a bearing on any decision of the Board of Patent Appeals and Interferences.

III. Status of the Claims

Claims 2 through 7 and 20 through 23 stand rejected under 35 U.S.C. 103 over Stein et al. (U.S. Patent No. 4,055,837, hereinafter *Stein*) and Howard (U.S. Patent No. 4,437,139, hereinafter *Howard*) and Dawson et al. (U.S. Patent No. 5,851,891, hereinafter *Dawson*).

IV. Status of Amendments

A first Office Action in the present application was mailed 11/05/2001. A first response with amendment was submitted by the appellants on 03/05/2002, and the amendment was entered. In response to appellants' first response with amendment, an Office Action with a Final Rejection was mailed 06/11/02. Appellants responded by submitting a Request for Continued Examination with amendment on 09/11/2002.

A non-final Office Action was mailed on 11/29/2002. Appellants responded by submitting a response with amendment on 02/28/2003. An Office Action with a Final Rejection was mailed 06/04/2003. Appellants filed a Notice of Appeal on 10/03/2003.

Appellants submit, concurrent with the present Appeal Brief, an amendment after final rejection under 37 CFR 1.116(b). Appellants submit that this amendment is responsive to objections raised in the Office Action mailed 06/04/2003, and therefore places the application in better form for appeal. These claims are reproduced in clean form in the Appendix of the present Appeal Brief.

V. Summary of the Invention

Appellants' disclosure describes a method and apparatus for improvements in a MOS transistor for use in as a decoupling capacitor in an integrated circuit. It is generally possible to connect a MOS transistor as a decoupling capacitor in two ways: connect the gate electrode to the minus power supply trace ("strong inversion mode") or connect the gate electrode to the positive power supply trace ("depletion mode"). This is shown in Figures 2 and 3, respectively. Generally the strong inversion mode configuration has proven the better of the two until recently. As the gate oxide layers have become thinner, leakage currents have become substantial.

Appellants' disclosure describes certain modifications in the structures and materials used in the fabrication of a MOS transistor that permit its use as a superior decoupling capacitor when used in the "depletion mode" circuit configuration. Generally this entails using a diffused gate region material with a reduced work function. Another modification that may be used is to heavily dope the substrate area. One embodiment's MOS transistor is shown in Figure 5, where the gate region 510 is fabricated from platinum silicide (PtSi). Other materials are also disclosed. See specification page 7 line 23 through page 8 line 4. When such a MOS transistor is connected in the "depletion mode" configuration, its performance may justify calling it a "weak inversion mode" capacitor as shown in Figure 6. The Figure 5 MOS transistor when configured as in Figure 6 has superior capacitance-to-voltage characteristics as shown in Figures 7 and 8. Specifically, curve 720 of Figure 7 shows how the "weak

inversion mode" capacitor actually increases in capacitance as the supply voltage decreases, an advantageous property for a decoupling capacitor.

VI. Issues

1. Whether claims 2 through 7 and 20 through 23 are unpatentable under 35 U.S.C. 103 over Stein et al. (U.S. Patent No. 4,055,837) and Howard (U.S. Patent No. 4,437,139) and Dawson et al. (U.S. Patent No. 5,851,891).

VII. Grouping of Claims (Independent Claims **Bolded**)

Group I: Decoupling Capacitor

For the purposes of this appeal claims **2**, 3, 4, 5, 6, 7, **20**, 21, 22, and 23 stand or fall together.

VIII. Argument

A. Claims 2 – 7 and 20 - 23 Are Not Obvious In View of Stein, Howard, and Dawson

Claims claims 2 through 7 and 20 through 23 stand rejected under 35 U.S.C. 103 over Stein et al. (U.S. Patent No. 4,055,837, hereinafter *Stein*) and Howard (U.S. Patent No. 4,437,139, hereinafter *Howard*) and Dawson et al. (U.S. Patent No. 5,851,891, hereinafter *Dawson*).

To establish a *prima facie* case of obviousness, case law as cited in the MPEP requires three criteria.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). MPEP § 706.02(j).

Moreover, the Federal Circuit has recently cautioned that the Patent Office must support its rejections for reasons that are stated on the record that establish why a particular combination would have been motivated by the prior art. It is inadequate to just state in conclusory fashion that just because two elements existed in the prior art, that

someone should have or would have been motivated to combine them. A specific teaching or a specific principle must be stated that makes the combination obvious.

> The need for specificity pervades this authority. See, e.g., In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) ("particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed"); In re Rouffet, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998) ("even when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination. In other words, the Board must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."); In re Fritch, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (the examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references"). In re Sang Su Lee, 277 F.3d 1338, 61 USPQ 1430 (Fed. Cir. 2002).

Appellants submit that (a) no specific showing of motivation to combine the references has been provided, and (b) that the references, even if combined, do not provide the claimed invention.

a. No Specific Showing of Motivation to Combine

The contention in the Final Office Action that it would be obvious to combine *Stein*, *Howard*, and *Dawson* is both legally and factually erroneous.

i. Factually, Stein does not suggest

Stein teaches a cell for use in non-volatile memory, including a MOS transistor 1 and a metal-nitride-oxide-semiconductor (MNOS)

capacitor 2 of Figures 1 and 3. The MOS transistor 1 of *Stein* is not connected as a decoupling capacitor as per the present invention: instead, the MOS transistor 1 of *Stein* is connected as an active switching device whose gate electrode is connected to a word line 10. Any special capacitance disclosed in *Stein* is embodied in MNOS capacitor 2. A MNOS capacitor is not a MOS transistor and hence is irrelevant to the present claimed invention. Enhancing the structure of MOS transistor 1 for use as a decoupling capacitor is not at issue in *Stein*, hence there is no intrinsic teaching that such enhancements would be useful.

The entirety of the explanation from the Office Action of why a MOS transistor with any desired gate work function should be added to *Stein* reads as follows:

> Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to make Stein's device with any desired gate work function as described by Dawson. (Dawson col. 2 line 49, Dawson in col. 4 lines 52-67 and col. 5 lines 1-15 also describes diffused gate material).

Final Office Action dated 06/04/2003, Page 4.

The Office Action makes no explanation whatsoever as to why the use of the chemical compounds purportedly disclosed in *Howard* would be useful when added to the MOS transistor 1 of *Stein*. As mentioned above, enhancing the structure of MOS transistor 1 for use as a decoupling capacitor is not at issue in *Stein*, hence there is no intrinsic teaching that such enhancements would be useful.

ii. Legally, burden not met

Furthermore, appellant submits that the evidentiary burden for an obviousness rejection has not been met. The Federal Circuit was specific in its admonitions in In re Sang Su Lee. Particular factual findings are required to underpin a §103 rejection. Here, the Final Office Action only makes the conclusory statement that "[t]herefore it would have been obvious to one of ordinary skill in the art at the time of the invention to make Stein's device with any desired gate work function as described by Dawson. (Dawson col. 2 line 49, Dawson in col. 4 lines 52-67 and col. 5 lines 1-15 also describes diffused gate material)."

No factual basis is given as to why someone would be motivated to add modifications to the MOS transistor of *Stein*, particularly in view of the fact that *Stein* used the MOS transistor 1 as an active switch controlled by a memory word line 10. What is the motivating factor? Moreover, motivation to combine the purported work function of *Dawson* or the PtSi of *Howard* to the MOS transistor of *Stein* as claimed in the present application is necessary. Without an evidentiary basis upon which to draw this conclusion, the conclusion cannot stand.

b. Even if Combined, *Stein*, *Howard*, and *Dawson* Do Not Meet the Claim Limitations

i. Group I

As discussed above, appellant submits that insufficient motivation exists to combine the *Stein*, *Howard*, and *Dawson* references. Even assuming, however, that such a combination is made, the combination itself does not include all of the elements and limitations of appellant's claims.

Claim 2 stands rejected as being anticipated by *Stein* and *Dawson*. The MOS transistor 1 of *Stein* discloses no "metallic gate electrode coupled to a .....positive power supply voltage trace" as recited in pertinent part in claim 2. Instead, the MOS transistor 1 of *Stein* is connected to a memory word line 10, which is a signal trace and not a power supply trace.

Claim 2 further recites in pertinent part "wherein said metal-oxide-semiconductor transistor includes the diffused gate region formed from material with a work function less than – 0.56 volts." In the Office Action, it is stated that "Dawson in col. 2 lines 48-50 describes the formation of IGFETs with any desired gate work function to form devices with low gate resistances." However, appellants have not found any such technical disclosure in *Dawson*. *Dawson* col. 2 lines 48-50 actually

recites "Accordingly, a *need exists* for a method of fabricating an IGFET that provides a low resistivity gate with the desired work function." (Appellants' emphasis added.) Appellants submit that this statement of a *need existing* is not an *enabling disclosure* of forming a gate with any *particular* work function. The only other use of the expression "work function" in *Dawson* occurs at col. 2, lines 19-20, which recites "Polysilicon, on the other hand, has a *known work function*..." And appellants' claimed invention is a *replacement for* the prior-art polysilicon used in a gate.

Claim 2 further recites in pertinent part "metallic source electrode and a metallic drain electrode coupled ... to each other and to a negative power supply voltage trace." Neither the MOS transistor 1 of *Stein* nor the various MOS transistors of *Dawson* show the drain connected to the source and both then connected to a negative power supply voltage trace. Indeed the MOS transistor 1 of *Stein* could not perform its switching function were this to be true.

Appellants submit that *Stein* and *Dawson* considered together do not disclose all of the claim elements and limitations of present claim 2. Therefore appellants submit that the invention claimed in claim 2 is not anticipated by *Stein* and *Dawson*, and therefore that claim 2 is allowable over the prior art of record.

Claim 3 stands rejected as being anticipated by, among others,

Howard. In the Office Action, a reference is made to *Howard* col. 3, line 31. However, appellants point out that the only place where *Howard* cites the use of platinum silicate (PtSi) is as part of *bottom electrode* 13, directly or indirectly coupled to the substrate 11. *Howard* does not show the use of platinum silicate as a "material of said diffused *gate region*" as recited in claim 3. Indeed, *Howard* only shows the use of platinum silicate in a bottom electrode 13 of a multi-layer capacitor 10 of Figure 1, not as a gate of a MOSFET. The multi-layer capacitor 10 of *Howard* requires a complicated dual-layer (or triple-layer) dialectric 14 consisting of a leakage prevention layer 18 and a high dielectric layer 17. This usage in *Howard* would if anything teach away from the use of platinum silicate in a more simple structure as disclosed in claim 3 of the present application. Because *Howard* does not teach the use of platinum silicate in a diffused gate region, and further because claim 3 depends from allowable claim 2, appellants submit that claim 3 is allowable over the prior art of record.

Claim 4 stands rejected as being anticipated by, among others, *Howard*. The Office Action states that the chemical compounds or elements tantalum nitrate (TaN), iridium (Ir), nickel (Ni), and arsenic (As) are disclosed in *Howard* at col. 3, lines 30-34. Appellants have downloaded a softcopy of *Howard* and performed word searches, but cannot find any reference to *any* of these compounds or elements in

Howard. Therefore appellants submit that the claimed invention of claim 4 is not anticipated by *Howard*. Since claim 4 depends from allowable claim 2, and further since claim 4 is not anticipated by *Howard*, appellants submit that claim 4 is allowable over the prior art of record.

Appellants point out that no separate rejections of claims 5, 6, and 7 were made in the Office Action. Appellants submit that claims 5, 6, and 7 are allowable as depending from allowable claim 2.

Claim 20 stands rejected as being anticipated by *Stein* and *Dawson*. Claim 20 recites in pertinent part "a metallic gate electrode coupled to a positive power supply voltage trace." In the Office Action, on page 4, it is stated that "Stein describes an apparatus including a metallic gate electrode to couple to a positive power supply voltage (Stein fig. 2)." Appellants again point out that the MOS transistor 1 of *Stein* has its gate electrode connected to the word line 10, which is a signal trace and not a power supply trace.

Claim 20 further recites in pertinent part "a diffused gate region formed from a material whose work function is less than minus 0.56 volts." In the Office Action, again on page 4, it is stated that "Dawson in col. 2 lines 48-50 describes the formation of IGFETs with any desired gate work function to form devices with low gate resistances." As mentioned above in connection with claim 2, appellants have not found any such technical disclosure in *Dawson*. *Dawson* col. 2 lines 48-50

actually recites "Accordingly, a *need exists* for a method of fabricating an IGFET that provides a low resistivity gate with the desired *work function*." (Appellants' emphasis added.) Appellants submit that this statement of a *need existing* is not an enabling disclosure of forming a gate with any particular work function. The only other use of the expression "work function" in *Dawson* occurs at col. 2, lines 19-20, which recites "Polysilicon, on the other hand, has a *known work function*..." And appellants' claimed invention is a *replacement for* the prior-art polysilicon used in a gate.

Appellants submit that *Stein* and *Dawson* considered together do not disclose all of the claim elements and limitations of present claim 20. Therefore appellants submit that the invention claimed in claim 20 is not anticipated by *Stein* and *Dawson*, and therefore that claim 20 is allowable over the prior art of record.

Claim 21 stands rejected as being anticipated by, among others, *Howard*. In the Office Action, a reference is made to *Howard* col. 3, line 31. However, as mentioned above in connection with claim 3, appellants point out that the only place where *Howard* cites the use of platinum silicate (PtSi) is as part of *bottom electrode* 13, directly or indirectly coupled to the substrate 11. *Howard* does not show "said material is platinum silicate" as recited in claim 21, referring to "a diffused gate region formed from a material" as recited in independent claim 20.

Indeed, *Howard* only shows the use of platinum silicate in a bottom electrode 13 of a multi-layer capacitor 10 of Figure 1, not as a gate of a MOSFET. The multi-layer capacitor 10 of *Howard* requires a complicated dual-layer (or triple-layer) dielectric 14 consisting of a leakage prevention layer 18 and a high dielectric layer 17. This usage in *Howard* would if anything teach away from the use of platinum silicate in a more simple structure as disclosed in claim 21 of the present application. Because *Howard* does not teach the use of platinum silicate in a diffused gate region, and further because claim 21 depends from allowable claim 20, appellants submit that claim 21 is allowable over the prior art of record.

Claim 22 stands rejected as being anticipated by, among others, *Howard*. The Office Action states that the chemical compounds or elements tantalum nitrate (TaN), iridium (Ir), nickel (Ni), and arsenic (As) are disclosed in *Howard* at col. 3, lines 30-34. As mentioned above in connection with claim 4, appellants have downloaded a softcopy of *Howard* and performed word searches, but cannot find any reference to *any* of these compounds or elements in *Howard*. Therefore appellants submit that the claimed invention of claim 22 is not anticipated by *Howard*. Since claim 22 depends from allowable claim 20, and further since claim 22 is not anticipated by *Howard*, appellants submit that claim 22 is allowable over the prior art of record.

Claim 23 stands rejected as being anticipated by, among others,

Stein. Since claim 23 depends from allowable claim 20, appellants submit that claim 23 is allowable over the prior art of record.

Appellants submit that all the claim elements and limitations of the pending claims are not disclosed in the combined *Stein*, *Howard*, and *Dawson* references. Therefore appellants submit that a proper *prima facie* case of obviousness has not been made out in the Office Action mailed 06/04/2003.

Conclusion

Appellants submit that all claims now pending are in condition for allowance. Such action is earnestly solicited at the earliest possible date. If there is a deficiency in fees, please charge our Deposit Acct. No. 02-2666.

Respectfully submitted,

Date: 19 November 2003

Dennis A. Nicholls, Reg. No. 42,036

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8598

IX. Appendix A: Claims Involved in Appeal (Clean Copy)

1. (Cancelled).

2. (Currently amended) An apparatus, comprising:

a metal-oxide-semiconductor transistor;

a metallic gate electrode coupled to a diffused gate region of said metal-oxide-semiconductor transistor and to a positive power supply voltage trace; and

a metallic source electrode and a metallic drain electrode coupled to said metal-oxide-semiconductor transistor and to each other and to a negative power supply voltage trace, wherein said metal-oxide-semiconductor transistor includes the diffused gate region formed from material with a work function less than – 0.56 volts.

3. (Previously amended) The apparatus of claim 2, wherein said material of said diffused gate region is platinum silicate.

4. (Previously amended) The apparatus of claim 2, wherein said material of said diffused gate region is selected from the group consisting of tantalum nitrate, iridium, nickel, and arsenic.

5. (Previously amended) The apparatus of claim 2, wherein said metal-oxide-semiconductor transistor includes a heavily-doped substrate area.

6. (Previously amended) The apparatus of claim 2, wherein said metal-oxide-semiconductor transistor is a p-channel device.

7. (Previously amended) The apparatus of claim 2, wherein said metal-oxide-transistor is an n-channel device.

8 through 19. (Cancelled)

20. (Currently amended) An apparatus, comprising:

a metallic gate electrode coupled to a positive power supply voltage trace;

a diffused gate region formed from a material whose work function is less than minus 0.56 volts coupled to said metallic gate electrode;

a gate insulator coupled to said diffused gate region;

a channel coupled to said gate insulator;

a diffused drain coupled to said channel; and

a diffused source coupled to said channel.

21. (Previously added) The apparatus of claim 20, wherein said material is platinum silicate.

22. (Previously added) The apparatus of claim 20, wherein said material is selected from the group consisting of tantalum nitrate, iridium, nickel, and arsenic.

23. (Previously added) The apparatus of claim 20, further comprising a substrate which is heavily-doped.

FIRST CLASS CERTIFICATE OF MAILING
(37 C.F.R. § 1.8(a))

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

on November 19, 2003.
Date of Deposit

Anne Collette
Name of Person Mailing Correspondence

Anne Collette — November 19, 2003
Signature — Date

Docket No.: 42390.P9239

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re the application of:	)	
	)	
Nair, Rajendran, et al.	)	
	)	
Serial No.: 09/677,698	)	Examiner: Rao, S.
	)	
Filed: 09/28/ 2000	)	Art Unit: 2814
	)	
For: METHOD AND APPARATUS FOR WEAK INVERSION MODE MOS DECOUPLING CAPACITOR	)	

APPELLANTS' BRIEF UNDER 37 CFR § 1.192
IN SUPPORT OF APPELLANTS' APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Hon. Commissioner for Patents
Mail Stop Appeal Brief – Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants hereby submit this Brief in triplicate in support of an appeal from a final decision of the Examiner, in the above-referenced case. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interference for allowance of the above-referenced patent application.

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There are no related appeals or interferences to appellants' knowledge that would have a bearing on any decision of the Board of Patent Appeals and Interferences.

III. Status of the Claims

Claims 2 through 7 and 20 through 23 stand rejected under 35 U.S.C. 103 over Stein et al. (U.S. Patent No. 4,055,837, hereinafter *Stein*) and Howard (U.S. Patent No. 4,437,139, hereinafter *Howard*) and Dawson et al. (U.S. Patent No. 5,851,891, hereinafter *Dawson*).

IV. Status of Amendments

A first Office Action in the present application was mailed 11/05/2001. A first response with amendment was submitted by the appellants on 03/05/2002, and the amendment was entered. In response to appellants' first response with amendment, an Office Action with a Final Rejection was mailed 06/11/02. Appellants responded by submitting a Request for Continued Examination with amendment on 09/11/2002.

A non-final Office Action was mailed on 11/29/2002. Appellants responded by submitting a response with amendment on 02/28/2003. An Office Action with a Final Rejection was mailed 06/04/2003. Appellants filed a Notice of Appeal on 10/03/2003.

Appellants submit, concurrent with the present Appeal Brief, an amendment after final rejection under 37 CFR 1.116(b). Appellants submit that this amendment is responsive to objections raised in the Office Action mailed 06/04/2003, and therefore places the application in better form for appeal. These claims are reproduced in clean form in the Appendix of the present Appeal Brief.

V. Summary of the Invention

Appellants' disclosure describes a method and apparatus for improvements in a MOS transistor for use in as a decoupling capacitor in an integrated circuit. It is generally possible to connect a MOS transistor as a decoupling capacitor in two ways: connect the gate electrode to the minus power supply trace ("strong inversion mode") or connect the gate electrode to the positive power supply trace ("depletion mode"). This is shown in Figures 2 and 3, respectively. Generally the strong inversion mode configuration has proven the better of the two until recently. As the gate oxide layers have become thinner, leakage currents have become substantial.

Appellants' disclosure describes certain modifications in the structures and materials used in the fabrication of a MOS transistor that permit its use as a superior decoupling capacitor when used in the "depletion mode" circuit configuration. Generally this entails using a diffused gate region material with a reduced work function. Another modification that may be used is to heavily dope the substrate area. One embodiment's MOS transistor is shown in Figure 5, where the gate region 510 is fabricated from platinum silicide (PtSi). Other materials are also disclosed. See specification page 7 line 23 through page 8 line 4. When such a MOS transistor is connected in the "depletion mode" configuration, its performance may justify calling it a "weak inversion mode" capacitor as shown in Figure 6. The Figure 5 MOS transistor when configured as in Figure 6 has superior capacitance-to-voltage characteristics as shown in Figures 7 and 8. Specifically, curve 720 of Figure 7 shows how the "weak

inversion mode" capacitor actually increases in capacitance as the supply voltage decreases, an advantageous property for a decoupling capacitor.

VI. Issues

1. Whether claims 2 through 7 and 20 through 23 are unpatentable under 35 U.S.C. 103 over Stein et al. (U.S. Patent No. 4,055,837) and Howard (U.S. Patent No. 4,437,139) and Dawson et al. (U.S. Patent No. 5,851,891).

VII. Grouping of Claims (Independent Claims **Bolded**)

Group I: Decoupling Capacitor

For the purposes of this appeal claims **2**, 3, 4, 5, 6, 7, **20**, 21, 22, and 23 stand or fall together.

VIII. Argument

A. Claims 2 – 7 and 20 - 23 Are Not Obvious In View of Stein, Howard, and Dawson

Claims claims 2 through 7 and 20 through 23 stand rejected under 35 U.S.C. 103 over Stein et al. (U.S. Patent No. 4,055,837, hereinafter *Stein*) and Howard (U.S. Patent No. 4,437,139, hereinafter *Howard*) and Dawson et al. (U.S. Patent No. 5,851,891, hereinafter *Dawson*).

To establish a *prima facie* case of obviousness, case law as cited in the MPEP requires three criteria.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). MPEP § 706.02(j).

Moreover, the Federal Circuit has recently cautioned that the Patent Office must support its rejections for reasons that are stated on the record that establish why a particular combination would have been motivated by the prior art. It is inadequate to just state in conclusory fashion that just because two elements existed in the prior art, that

someone should have or would have been motivated to combine them. A specific teaching or a specific principle must be stated that makes the combination obvious.

> The need for specificity pervades this authority. See, e.g., In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) ("particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed"); In re Rouffet, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998) ("even when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination. In other words, the Board must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."); In re Fritch, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (the examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references"). In re Sang Su Lee, 277 F.3d 1338, 61 USPQ 1430 (Fed. Cir. 2002).

Appellants submit that (a) no specific showing of motivation to combine the references has been provided, and (b) that the references, even if combined, do not provide the claimed invention.

a. No Specific Showing of Motivation to Combine

The contention in the Final Office Action that it would be obvious to combine *Stein*, *Howard*, and *Dawson* is both legally and factually erroneous.

i. Factually, Stein does not suggest

Stein teaches a cell for use in non-volatile memory, including a MOS transistor 1 and a metal-nitride-oxide-semiconductor (MNOS)

capacitor 2 of Figures 1 and 3. The MOS transistor 1 of *Stein* is not connected as a decoupling capacitor as per the present invention: instead, the MOS transistor 1 of *Stein* is connected as an active switching device whose gate electrode is connected to a word line 10. Any special capacitance disclosed in *Stein* is embodied in MNOS capacitor 2. A MNOS capacitor is not a MOS transistor and hence is irrelevant to the present claimed invention. Enhancing the structure of MOS transistor 1 for use as a decoupling capacitor is not at issue in *Stein*, hence there is no intrinsic teaching that such enhancements would be useful.

The entirety of the explanation from the Office Action of why a MOS transistor with any desired gate work function should be added to *Stein* reads as follows:

> Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to make Stein's device with any desired gate work function as described by Dawson. (Dawson col. 2 line 49, Dawson in col. 4 lines 52-67 and col. 5 lines 1-15 also describes diffused gate material).

Final Office Action dated 06/04/2003, Page 4.

The Office Action makes no explanation whatsoever as to why the use of the chemical compounds purportedly disclosed in *Howard* would be useful when added to the MOS transistor 1 of *Stein*. As mentioned above, enhancing the structure of MOS transistor 1 for use as a decoupling capacitor is not at issue in *Stein*, hence there is no intrinsic teaching that such enhancements would be useful.

ii. Legally, burden not met

Furthermore, appellant submits that the evidentiary burden for an obviousness rejection has not been met. The Federal Circuit was specific in its admonitions in In re Sang Su Lee. Particular factual findings are required to underpin a §103 rejection. Here, the Final Office Action only makes the conclusory statement that "[t]herefore it would have been obvious to one of ordinary skill in the art at the time of the invention to make Stein's device with any desired gate work function as described by Dawson. (Dawson col. 2 line 49, Dawson in col. 4 lines 52-67 and col. 5 lines 1-15 also describes diffused gate material)."

No factual basis is given as to why someone would be motivated to add modifications to the MOS transistor of *Stein*, particularly in view of the fact that *Stein* used the MOS transistor 1 as an active switch controlled by a memory word line 10. What is the motivating factor? Moreover, motivation to combine the purported work function of *Dawson* or the PtSi of *Howard* to the MOS transistor of *Stein* as claimed in the present application is necessary. Without an evidentiary basis upon which to draw this conclusion, the conclusion cannot stand.

b. Even if Combined, *Stein*, *Howard*, and *Dawson* Do Not Meet the Claim Limitations

i. Group I

As discussed above, appellant submits that insufficient motivation exists to combine the *Stein*, *Howard*, and *Dawson* references. Even assuming, however, that such a combination is made, the combination itself does not include all of the elements and limitations of appellant's claims.

Claim 2 stands rejected as being anticipated by *Stein* and *Dawson*. The MOS transistor 1 of *Stein* discloses no "metallic gate electrode coupled to a .....positive power supply voltage trace" as recited in pertinent part in claim 2. Instead, the MOS transistor 1 of *Stein* is connected to a memory word line 10, which is a signal trace and not a power supply trace.

Claim 2 further recites in pertinent part "wherein said metal-oxide-semiconductor transistor includes the diffused gate region formed from material with a work function less than – 0.56 volts." In the Office Action, it is stated that "Dawson in col. 2 lines 48-50 describes the formation of IGFETs with any desired gate work function to form devices with low gate resistances." However, appellants have not found any such technical disclosure in *Dawson*. *Dawson* col. 2 lines 48-50 actually

recites "Accordingly, a *need exists* for a method of fabricating an IGFET that provides a low resistivity gate with the desired work function." (Appellants' emphasis added.) Appellants submit that this statement of a *need existing* is not an *enabling disclosure* of forming a gate with any *particular* work function. The only other use of the expression "work function" in *Dawson* occurs at col. 2, lines 19-20, which recites "Polysilicon, on the other hand, has a *known work function...*" And appellants' claimed invention is a *replacement for* the prior-art polysilicon used in a gate.

Claim 2 further recites in pertinent part "metallic source electrode and a metallic drain electrode coupled ... to each other and to a negative power supply voltage trace." Neither the MOS transistor 1 of *Stein* nor the various MOS transistors of *Dawson* show the drain connected to the source and both then connected to a negative power supply voltage trace. Indeed the MOS transistor 1 of *Stein* could not perform its switching function were this to be true.

Appellants submit that *Stein* and *Dawson* considered together do not disclose all of the claim elements and limitations of present claim 2. Therefore appellants submit that the invention claimed in claim 2 is not anticipated by *Stein* and *Dawson*, and therefore that claim 2 is allowable over the prior art of record.

Claim 3 stands rejected as being anticipated by, among others,

Howard. In the Office Action, a reference is made to *Howard* col. 3, line 31. However, appellants point out that the only place where *Howard* cites the use of platinum silicate (PtSi) is as part of *bottom electrode* 13, directly or indirectly coupled to the substrate 11. *Howard* does not show the use of platinum silicate as a "material of said diffused *gate region*" as recited in claim 3. Indeed, *Howard* only shows the use of platinum silicate in a bottom electrode 13 of a multi-layer capacitor 10 of Figure 1, not as a gate of a MOSFET. The multi-layer capacitor 10 of *Howard* requires a complicated dual-layer (or triple-layer) dialectric 14 consisting of a leakage prevention layer 18 and a high dielectric layer 17. This usage in *Howard* would if anything teach away from the use of platinum silicate in a more simple structure as disclosed in claim 3 of the present application. Because *Howard* does not teach the use of platinum silicate in a diffused gate region, and further because claim 3 depends from allowable claim 2, appellants submit that claim 3 is allowable over the prior art of record.

Claim 4 stands rejected as being anticipated by, among others, *Howard*. The Office Action states that the chemical compounds or elements tantalum nitrate (TaN), iridium (Ir), nickel (Ni), and arsenic (As) are disclosed in *Howard* at col. 3, lines 30-34. Appellants have downloaded a softcopy of *Howard* and performed word searches, but cannot find any reference to *any* of these compounds or elements in

Howard. Therefore appellants submit that the claimed invention of claim 4 is not anticipated by *Howard*. Since claim 4 depends from allowable claim 2, and further since claim 4 is not anticipated by *Howard*, appellants submit that claim 4 is allowable over the prior art of record.

Appellants point out that no separate rejections of claims 5, 6, and 7 were made in the Office Action. Appellants submit that claims 5, 6, and 7 are allowable as depending from allowable claim 2.

Claim 20 stands rejected as being anticipated by *Stein* and *Dawson*. Claim 20 recites in pertinent part "a metallic gate electrode coupled to a positive power supply voltage trace." In the Office Action, on page 4, it is stated that "Stein describes an apparatus including a metallic gate electrode to couple to a positive power supply voltage (Stein fig. 2)." Appellants again point out that the MOS transistor 1 of *Stein* has its gate electrode connected to the word line 10, which is a signal trace and not a power supply trace.

Claim 20 further recites in pertinent part "a diffused gate region formed from a material whose work function is less than minus 0.56 volts." In the Office Action, again on page 4, it is stated that "Dawson in col. 2 lines 48-50 describes the formation of IGFETs with any desired gate work function to form devices with low gate resistances." As mentioned above in connection with claim 2, appellants have not found any such technical disclosure in *Dawson*. *Dawson* col. 2 lines 48-50

actually recites "Accordingly, a *need exists* for a method of fabricating an IGFET that provides a low resistivity gate with the desired *work function.*" (Appellants' emphasis added.) Appellants submit that this statement of a *need existing* is not an enabling disclosure of forming a gate with any particular work function. The only other use of the expression "work function" in *Dawson* occurs at col. 2, lines 19-20, which recites "Polysilicon, on the other hand, has a *known work function...*" And appellants' claimed invention is a *replacement for* the prior-art polysilicon used in a gate.

Appellants submit that *Stein* and *Dawson* considered together do not disclose all of the claim elements and limitations of present claim 20. Therefore appellants submit that the invention claimed in claim 20 is not anticipated by *Stein* and *Dawson*, and therefore that claim 20 is allowable over the prior art of record.

Claim 21 stands rejected as being anticipated by, among others, *Howard*. In the Office Action, a reference is made to *Howard* col. 3, line 31. However, as mentioned above in connection with claim 3, appellants point out that the only place where *Howard* cites the use of platinum silicate (PtSi) is as part of *bottom electrode* 13, directly or indirectly coupled to the substrate 11. *Howard* does not show "said material is platinum silicate" as recited in claim 21, referring to "a diffused gate region formed from a material" as recited in independent claim 20.

Indeed, *Howard* only shows the use of platinum silicate in a bottom electrode 13 of a multi-layer capacitor 10 of Figure 1, not as a gate of a MOSFET. The multi-layer capacitor 10 of *Howard* requires a complicated dual-layer (or triple-layer) dialectric 14 consisting of a leakage prevention layer 18 and a high dielectric layer 17. This usage in *Howard* would if anything teach away from the use of platinum silicate in a more simple structure as disclosed in claim 21 of the present application. Because *Howard* does not teach the use of platinum silicate in a diffused gate region, and further because claim 21 depends from allowable claim 20, appellants submit that claim 21 is allowable over the prior art of record.

Claim 22 stands rejected as being anticipated by, among others, *Howard*. The Office Action states that the chemical compounds or elements tantalum nitrate (TaN), iridium (Ir), nickel (Ni), and arsenic (As) are disclosed in *Howard* at col. 3, lines 30-34. As mentioned above in connection with claim 4, appellants have downloaded a softcopy of *Howard* and performed word searches, but cannot find any reference to *any* of these compounds or elements in *Howard*. Therefore appellants submit that the claimed invention of claim 22 is not anticipated by *Howard*. Since claim 22 depends from allowable claim 20, and further since claim 22 is not anticipated by *Howard*, appellants submit that claim 22 is allowable over the prior art of record.

Claim 23 stands rejected as being anticipated by, among others,

Stein. Since claim 23 depends from allowable claim 20, appellants submit that claim 23 is allowable over the prior art of record.

Appellants submit that all the claim elements and limitations of the pending claims are not disclosed in the combined *Stein*, *Howard*, and *Dawson* references. Therefore appellants submit that a proper *prima facie* case of obviousness has not been made out in the Office Action mailed 06/04/2003.

Conclusion

Appellants submit that all claims now pending are in condition for allowance. Such action is earnestly solicited at the earliest possible date. If there is a deficiency in fees, please charge our Deposit Acct. No. 02-2666.

Respectfully submitted,

Date: 19 November 2003

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IX. Appendix A: Claims Involved in Appeal (Clean Copy)

1. (Cancelled).

2. (Currently amended) An apparatus, comprising:

a metal-oxide-semiconductor transistor;

a metallic gate electrode coupled to a diffused gate region of said metal-oxide-semiconductor transistor and to a positive power supply voltage trace; and

a metallic source electrode and a metallic drain electrode coupled to said metal-oxide-semiconductor transistor and to each other and to a negative power supply voltage trace, wherein said metal-oxide-semiconductor transistor includes the diffused gate region formed from material with a work function less than – 0.56 volts.

3. (Previously amended) The apparatus of claim 2, wherein said material of said diffused gate region is platinum silicate.

4. (Previously amended) The apparatus of claim 2, wherein said material of said diffused gate region is selected from the group consisting of tantalum nitrate, iridium, nickel, and arsenic.

5. (Previously amended) The apparatus of claim 2, wherein said metal-oxide-semiconductor transistor includes a heavily-doped substrate area.

6. (Previously amended) The apparatus of claim 2, wherein said metal-oxide-semiconductor transistor is a p-channel device.

7. (Previously amended) The apparatus of claim 2, wherein said metal-oxide-transistor is an n-channel device.

8 through 19. (Cancelled)

20. (Currently amended) An apparatus, comprising:

a metallic gate electrode coupled to a positive power supply voltage trace;

a diffused gate region formed from a material whose work function is less than minus 0.56 volts coupled to said metallic gate electrode;

a gate insulator coupled to said diffused gate region;

a channel coupled to said gate insulator;

a diffused drain coupled to said channel; and

a diffused source coupled to said channel.

21. (Previously added) The apparatus of claim 20, wherein said material is platinum silicate.

22. (Previously added) The apparatus of claim 20, wherein said material is selected from the group consisting of tantalum nitrate, iridium, nickel, and arsenic.

23. (Previously added) The apparatus of claim 20, further comprising a substrate which is heavily-doped.